AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings.

Listing of Claims:

1. (Canceled)

2. (Canceled)

3. (Previously Presented) A method for forming a semiconductor device, comprising:

forming an insulation layer in a capacitor region and a metal interconnection region over a substrate;

forming a first trench in the insulation layer of the capacitor region and the metal interconnection region;

forming a first barrier metal and a first metal interconnection inside the first trench;

forming a second trench by selectively etching the insulation layer around the first barrier metal of the capacitor region;

forming a third trench in the first barrier metal by selectively etching the first metal interconnection of the capacitor region; and

forming a capacitor in the second and third trenches; and

wherein the capacitor and the first metal interconnection are formed in the same layer.

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Previously Presented) A method for fabricating a semiconductor device, comprising:

forming a first and a second insulation layers in the capacitor region and the metal interconnection region over a substrate formed with a lower conductive layer;

forming an interconnection trench in the metal interconnection region, a first trench in the capacitor region, and a via hole connected to the lower conductive layer by selectively etching the insulation layer;

forming a copper interconnection, a first copper interconnection and a via contact plug by forming a first copper layer in the interconnection trench, the via hole and the first trench;

forming a second trench by selectively etching the second insulation layer of the capacitor region;

forming a capacitor in the second trench; and

forming a barrier layer on the capacitor and a second copper interconnection on the barrier layer.

9. (Original) The method as recited in claim 8, wherein the insulation layer includes an etching blocking layer between the first insulation layer and the second insulation layer.

10. (Original) The method as recited in claim 8, further including a hard mask on the second insulation layer.

11. (Previously Presented) The method as recited in claim 8, wherein forming the interconnection trench further comprises forming the interconnection trench and the first trench simultaneously prior to forming the via hole.

12. (Previously Presented) The method as recited in claim 8, wherein forming the interconnection trench forming the via hole first, and then forming the interconnection trench and the first trench simultaneously.

13. (Original) The method as recited in claim 8, wherein the first and the second copper conductive layers use a reflow method after forming a layer in a sputtering method, a CVD method or an electroplating method.

14. (Original) The method as recited in claim 8, wherein in case of using the electroplating method, a seed layer is formed in a method selected from a group of a physical vapor deposition (PVD), a chemical vapor deposition (CVD) and an electroless deposition, or a combination thereof.

15. (Previously Presented) The method as recited in claim 8, further including forming a first barrier metal prior to the first copper layer.

16. (Previously Presented) A method for fabricating a semiconductor device, comprising:

forming an insulation layer in a metal interconnection region and a capacitor region over a substrate formed with a lower conductive layer;

forming an interconnection trench in the metal interconnection region, a first trench in the capacitor region and a via hole by selectively etching the insulation layer;

forming a copper interconnection, a via contact plug and a first copper interconnection by forming a first barrier metal and a first copper layer in the interconnection trench, the via hole and the first trench;

forming a second trench by selectively etching the insulation layer around the first copper interconnection in the capacitor region;

forming a third trench in the first barrier metal by selectively etching the first copper interconnection;

forming a capacitor in the second and the third trenches; and

forming a second copper interconnection by forming a second copper layer on the capacitor.

17. (Original) The method as recited in claim 16, wherein a second barrier metal is formed prior to the formation of the second copper layer.

18. (Previously Presented) The method as recited in claim 17, wherein the first and the second barrier metals includes one selected from a group of Ta, TaN, TiN, WN, TaC, WC, TiSiN and TaSiN, and a combination thereof.

19. (Previously Presented) The method as recited in claim 3, wherein the first metal interconnection includes copper.

20. (Previously Presented) The method as recited in claim 3, wherein the capacitor includes first and second electrodes are of a metal selected from a group of Pt, Ru, Ir and W.

21. (Previously Presented) The method as recited in claim 3, wherein the capacitor includes a dielectric layer of an oxide selected from a group of Ta oxide, Ba-Sr-Ti oxide, Zr oxide, Hf oxide, Pb-Zn-Ti oxide, Sr-Bi-Ta oxide, and a combination thereof.